IN THE CLAIMS

No amendments have been made to the claims. This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A method comprising:

forming a thin film stack on a substrate, wherein the thin film stack includes at least a polysilicon layer and an oxide layer;

forming a hardmask layer on the thin film stack;

forming an anti-reflective coating (ARC) layer on the hardmask layer;

patterning the ARC layer;

etching the hardmask layer using the patterned ARC layer as a mask; and

etching the thin film stack using the hardmask layer as a mask.

2. (Original) 193nm or less lithography.

3. (Original) The method of claim 2, wherein the thickness of the resist is less than 5000Å.

4. (Original) The method of claim 3, wherein the hardmask layer has a thickness of between 1000 and 3000Å and the ARC layer has a thickness of between 100 and 500Å.

5. (Original) The method of claim 3, wherein the hardmask layer comprises a material that has high selectivity to both polysilicon and oxide etch chemistries.

6. (Original) The method of claim 3, wherein the hardmask layer comprises amorphous carbon.

7. (Original) The method of claim 6, wherein the hardmask layer comprises Applied Materials® Advanced Patterning Film™ (APF™).

8. (Original) The method of claim 3, wherein the ARC layer is removed during the etching of the thin film stack.

9. (Original) The method of claim 3, further comprising removing the hardmask material from the thin film stack.

10. (Original) A method comprising:
forming a flash memory gate stack on a substrate;
forming a hardmask layer on the flash memory gate stack;
forming an anti-reflective coating (ARC) layer on the hardmask layer;
patterning the ARC layer;
etching the hardmask layer using the patterned ARC layer as a mask; and
etching the flash memory gate stack using the hardmask layer as a mask.

11. (Original) The method of claim 10, wherein the ARC layer is patterned with resist using 193nm or less lithography.

12. (Original) The method of claim 11, wherein the thickness of the resist is less than 5000Å.

13. (Original) The method of claim 12, wherein the flash memory gate stack is comprised of a gate dielectric layer, a floating gate layer, an inter-electrode dielectric layer, and a control gate electrode layer.

14. (Original) The method of claim 12, wherein the hardmask layer has a thickness of between 1000 and 3000Å and the ARC layer has a thickness of between 100 and 500Å.

15. (Original) The method of claim 12, wherein the hardmask layer comprises a material that has high selectivity to both polysilicon and oxide etch chemistries.

16. (Original) The method of claim 12, wherein the hardmask layer comprises amorphous carbon.

17. (Original) The method of claim 16, wherein the hardmask layer comprises Applied Materials® Advanced Patterning Film™ (APF™).

18. (Original) The method of claim 12, wherein the ARC layer is removed during the etching of the flash memory gate stack.

19. (Original) The method of claim 12, further comprising removing the hardmask material from the flash memory gate stack.

20 - 30. (Canceled)